



Training Workshop

“Thematic and Hands-on Support for participation in FP7 ICT Call 7”

Moldavian Priorities in ICT Work Program 2011-2012:

3.4. Computing Systems

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1. Introduction (1)

Computing is the main enabling technology that has radically changed the economy over the last 20 years.

The contribution of ICT sector to the annual labor productivity growth in the period of 1995-2004 years was of: 44,7% - in Korea; 42,3% – in Japan, and 41% - in Ireland.

Informatics networks, mainly Internet, by enforcing communication and data processing facilities, radically improved the modalities of doing business and the quality of human life.

In the future all interested “objects” (computers, cars, offices, appartements, unwells, veggies, etc.) can be, if needed, controled/monitored online via informatics networks.

These requires the integration of embedded, general-purpose, mobile and high-performance computing.



1. Introduction (2)

Many years advances in computing have been driven by the increase of the speed as well as architectural improvements of microprocessors.

Today, simply speeding up clocks becomes very expensive and leads to excessive power consumption.

It is easier and cheaper to put several processors on a chip rather than designing a processor to span the whole chip.

Although it is relatively straightforward to put lots of cores on a chip, this leads to the problem of trying to program it in order to get the benefits from the parallelism.

Because of different functions and the discrete character of the processor performance, more efficient is the emergence of multiple, heterogeneous and interconnected processing elements on a single chip.

This emergence requires a radical change in computing architectures and programming paradigms – aspects of research in FP7 research theme “3.4 Computing Systems”.

Already in 2013, laptops are expected to have 4 to 8 cores, workstations 8 to 16 cores and servers 16 to 32 cores per chip or even more in case of enterprise servers.

2. Overview of ICT WP 2011-2012: “3.4 Computing Systems” (1)

2.1. Objective of research theme Computing Systems

- transition to multicore architectures across the whole computing spectrum: embedded, general-purpose (PC/servers) and high-performance (HPC) computing;
- transition affects the underlying hardware, the system software (compilers, tools, OS, etc) and the programming paradigms.

2.2. Motivation

- to leverage on the strong European position in embedded computing in order to improve the European position in general-purpose and highperformance computing.

2. Overview of ICT WP 2011-2012: “3.4 Computing Systems” (2)

2.3. Target outcomes

a) Parallel and Concurrent Computing

- Automatic parallelisation, new high-level parallel & concurrent programming languages and/or extensions to existing languages that provide portable performance.
- Projects should go beyond on-chip, off-chip boundaries addressing the challenges of programming, testing, verification and debugging, performance monitoring and analysis, low-power and power management especially for large scale parallel systems and data centres, and heterogeneous and accelerator-based multicore systems.
- Research priorities include:
 - domainspecific languages;
 - concurrent algorithms and transformation of concurrency to parallelism through adaptive compilers and runtime systems;
 - new verification and optimisation environments for parallel software;
 - efficient execution exploiting heterogeneous cores;
 - new approaches to scalability of high-performance computing application codes.

2. Overview of ICT WP 2011-2012: “3.4 Computing Systems” (3)

2.3. Target outcomes

b) Virtualisation

- Virtualisation technologies that are ensuring task isolation and optimised resource allocation as well as guaranteeing performance, timing and reliability constraints.
- The focus is on full virtualisation solutions for heterogeneous multicore platforms including the design of virtualisation-ready heterogeneous multicore hardware platforms and support for accelerator virtualisation.

c) Customisation

- Unifying hardware design and software development with emphasis on rapid discovery and production of optimal customisations of heterogeneous single-chip multicore systems and associated tool-chains for particular applications.
- Research priorities include:
 - reconfigurable, flexible, soft or hybrid architectures and instruction sets;
 - automatic tool-chain generation;
 - system modelling and simulation, including performance predictability;
 - efficient exploration of the customisation space;
 - low-power and customisation for power efficiency;
 - parallel programming for single-chip multicore architectures;
 - architectural and system-level reliability techniques to counter increasingly probabilistic behaviour of transistors in lower geometries.

2. Overview of ICT WP 2011-2012: “3.4 Computing Systems” (4)

2.3. Target outcomes

d) Architecture and Technology

- The focus is on the impact of next-generation chip fabrication technology on system architectures, tools and compilers.
- Research areas include:
 - implications of 3D stacking;
 - alternative (non von Neumann) models of computation.
- The key **challenge** is to bridge parallel computing architectures and chip fabrication technology.

e) International Collaboration

- The purpose is to analyse international research agendas and to prepare concrete initiatives for international collaboration, for all topics of this objective, in particular with: USA, India, China and Latin America.
- Separate proposals per geographic area are expected.

2. Overview of ICT WP 2011-2012: "3.4 Computing Systems" (5)

2.4. Expected Impact

- Drastically improved programmability of future parallel multicore/multichip computing systems, providing efficient execution and portable performance of codes on a large variety of computing platforms;
- Efficient and ubiquitous use of virtualisation for heterogeneous multi-cores;
- Accelerated system development and production, enabling new products to be realised with a considerably shorter time-to-market;
- Reinforced European excellence in multi-core computing architectures, system software and tools;
- Strengthened European leadership in cross-cutting technologies that are applicable to different market segments of computing systems and, in particular, European leadership in parallel computing systems for large data centres.



2. Overview of ICT WP 2011-2012: “3.4 Computing Systems” (6)

2.5. Funding schemes

- (1.2a-1.2d): STREP, NoE
- (1.2e): CSA

STREP – Small or medium-scale focused research actions (a specific research objective in a sharply focused approach; support to research projects carried out by consortia with at least three ‘legal entities’ established in different EU Member States or Associated countries).

NoE – Networks of Excellence (support to a *Joint Programme of Activities* implemented by a number of research organisations integrating their activities in a given field, carried out by research teams in the framework of longer term cooperation).

CSA – Coordination and support actions (Support to activities aimed at coordinating or supporting research activities and policies: networking, exchanges, trans-national access to research infrastructures, studies, conferences, etc).

2.6. Indicative budget distribution of the total €45 million

- **STREP: €40 million**
- **NoE: €4 million**
- **CSA: €1 million**



2. Overview of ICT WP 2011-2012: “3.4 Computing Systems” (7)

2.7. Call 7 (FP7-ICT-2011-7)

Open 28 Sept 2010

Close 18 Jan 2011

Projects starting mid 2011 & ending 2014.

Objective Coordinator: Dr. Panagiotis Tsarchopoulos,
European Commission, Belgium



3. Proposals preparation outline

Analysis of previous Call projects in Computing Systems:

- projects within FP6 (2002-2006);
- projects within FP7, 2007 Call;
- projects within FP7, 2009 Call.

Details about the requirements of the 2010 Call (Call 7).

Particularities of the participation of Moldavian researchers in projects within 2010 Call.

4. Projects in Computing within FP6 (2002-2006)

- 40 projects, including:
 - 8 Integrated Projects (IP);
 - 3 Networks of Excellence projects (NoE);
 - 23 Strategic Targeted Research Projects (STREP);
 - a number of support/coordination actions.

- Covered areas:
 - System design;
 - Computing;
 - Co-operating Objects and Wireless Sensor Networks;
 - Middleware;
 - Control Systems;
 - Embedded support activities.

- Total funding - €146 million.



5. FP7 “3.4. Computing System’s” projects (1)

5.1. Overview

- **2 former Calls:** 2007 (Call 1), 2009 (Call 4).
- **Funding** - €25 million per Call.
- **Project Portfolio:** 1 NoE, 1 SA, 17 STREP (8 from Call 1; 9 from Call 4)
- **Three main constraints:**
 - Research on parallelisation and programmability should keep a focus on **single-chip** multicore systems;
 - Projects should adopt a holistic approach taking into account hardware, systems software and parallel programming;
 - Projects should address **cross-cutting** technologies applicable to all market segments of computing (embedded, general-purpose and high performance).

Source: *Dr. Panagiotis Tsarchopoulos, European Research in Computing Systems, 28.09.2010*



5. FP7 “3.4. Computing System’s” projects (2)

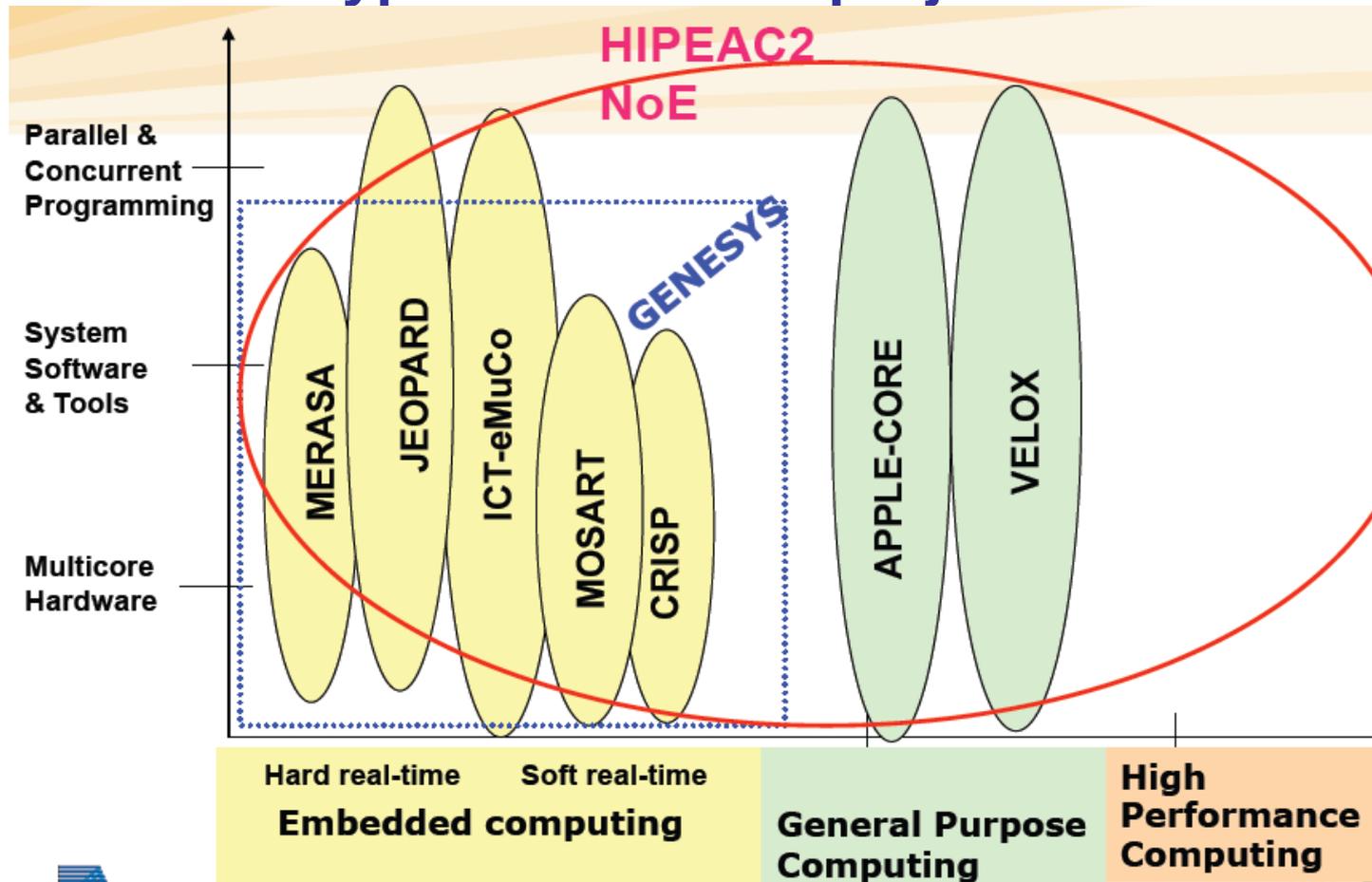
5.2. 2007 Call proposals

Received proposals	Above threshold	Funding
31	24	9

Very high quality of received proposals: 77% above threshold.

5. FP7 “3.4. Computing System’s” projects (3)

5.3. 2007 Call types of retained projects





5. FP7 “3.4. Computing System’s” projects (4)

Project title (2007 Call)	Funding, € mln	Cost, € mln	Nr. of particip.	Start date	Duration, months	Contract Type
Generic embedded system platform (GENESYS)	1.85	2.79	24	2008-01-01	18	STREP
High performance and embedded architecture and compilation (HiPEAC)	4.8	5.57	11	2008-02-01	48	NoE
Embedded multi-core processing for mobile communication systems (ICT-EMUCO)	2.9	4.56	7	2008-02-01	24	STREP
Multi-core execution of hard-real-time applications supporting analysability (MERASA)	2.1	3.0	5	2007-11-01	36	STREP
Mapping optimization for scalable multi-core architecture (MOSART)	3.1	4.47	7	2008-01-01	36	STREP
Architecture paradigms and programming languages for efficient programming of multiple CORES (APPLE-CORE)	2.1	2.75	5	2007-11-01	36	STREP
Cutting edge reconfigurable ics for stream processing (CRISP)	2.8	4.4	6	2008-01-01	36	STREP
Java environment for parallel realtime development (JEOPARD)	2.4	3.35	9	2008-01-01	30	STREP
Velox: an integrated approach to transactional memory on multi- and many-core computers (VELOX)	3.09	4.45	8	2008-01-01	36	STREP



5. FP7 “3.4. Computing System’s” projects (5)

5.4. 2009 Call target outcomes

5.4.1. STREPs projects target outcomes (€24.7 million)

- a) Parallelisation and Programmability;
- b) Continuous Adaptation, Virtualisation, Customisation;
- c) System Simulation and Analysis;
- d) Technology Implications (3D).

5.4.2. CSAs projects target outcomes (€0.3 million)

- e) R&D agenda in High-Performance Computing

5. FP7 “3.4. Computing System’s” projects (6)

5.5. 2009 Call proposals

Funding scheme (target outcomes)	Received proposals	Above threshold	Retained/ Reserve
STREP (a-d)	40	29	9/1
CSA (e)	2	1	1/0

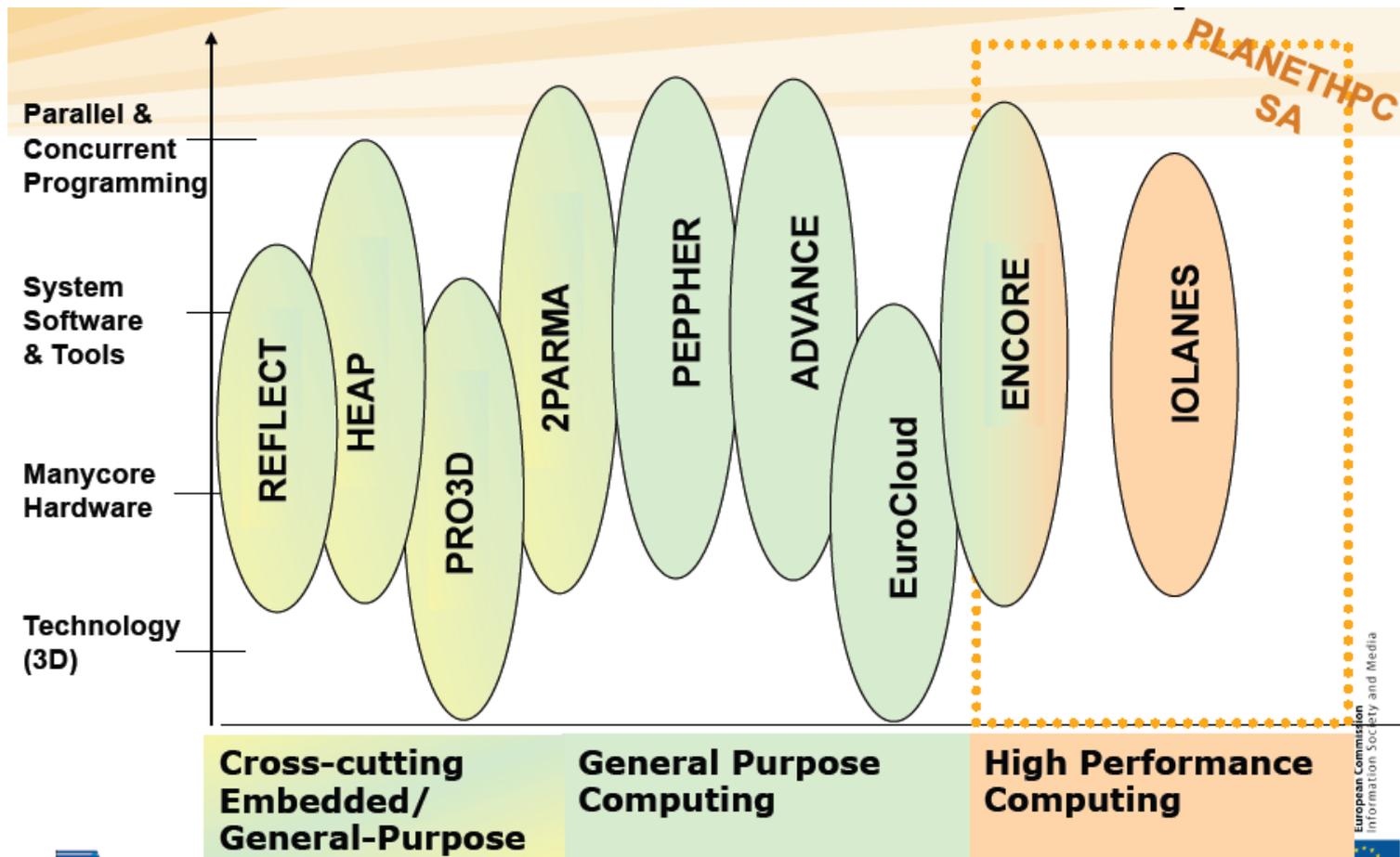
30% more proposals received than in 2007 Call (2007 Call: 31; 2009 Call: 42)

Very high quality of received proposals: every 3 out of 4 proposals scored above threshold

Source: *Dr. Panagiotis Tsarchopoulos, European Research in Computing Systems, 28.09.2010*

5. FP7 “3.4. Computing System’s” projects (7)

5.6. 2009 Call types of retained projects



5. FP7 “3.4. Computing System’s” projects (8)

Project title (2009 Call)	Funding, € mln	Cost, € mln	Nr. of particip.	Start date	Duration, months	Contract Type
Rendering <u>FPGAs</u> to Multi-Core Embedded Computing (REFLECT)	2.72	3.70	8	2010-01-01	36	STREP
A highly efficient adaptive multi-processor framework (HEAP)	2.22	3.32	9	2010-02-01	33	STREP
Programming for Future 3D Architectures with Many Cores (PRO3D)	2.62	3.54	6	2010-01-01	30	STREP
<u>PAR</u>allel <u>PAR</u>adigms and Run-time <u>MAN</u>agement techniques for Many-core Architectures (2PARMA)	2.74	3.99	7	2010-01-01	36	STREP
Performance Portability and Programmability for Heterogeneous Many-core Architectures (PEPHER)	2.55	3.44	8	2010-01-01	36	STREP
Asynchronous and Dynamic <u>Virtualisation</u> through performance <u>AN</u>alysis to support Concurrency Engineering (ADVANCE)	3.11	4.56	9	2010-02-01	36	STREP
Energy-conscious 3D Server-on-Chip for Green Cloud Services (<u>EuroCloud</u>)	3.29	5.44	5	2010-01-01	36	STREP
<u>EN</u>abling technologies for a programmable many-CORE (ENCORE)	2.53	3.55	6	2010-03-01	36	STREP
Advancing the Scalability and Performance of I/O Subsystems in Multi-core Platforms (IOLANES)	2.72	4.26	6	2010-01-01	36	STREP

6. FP7 “3.4. Computing System’s” 2010 Call target outcomes

- a) Parallel & Concurrent Computing
 - Multicore, multichip (beyond single-chip)
 - Parallel/concurrent software & tools
- b) Virtualisation
 - Heterogeneous multicore systems
- c) Customisation
 - Reconfigurable architectures
 - Multicore on single-chip
 - Tool-chains
 - System modelling & simulation
- d) Architecture & Technology
 - 3D stacking
 - Alternative computation models
- e) International collaboration

STREPs (40m)

NoE (4m)

CSAs (1m)

Source: Dr. P.Tsarchopoulos, European Research in Computing Systems, 28.09.2010

7. Opportunities in the field for Moldavian researchers



Research aspects	Readiness	
	now	near future
a) Parallel and Concurrent Computing:		
- domainspecific languages	?	yes
- concurrent algorithms and transformation of concurrency to parallelism through adaptive compilers and runtime systems	yes	yes
- new verification and optimisation environments for parallel software	?	yes
- efficient execution exploiting heterogeneous cores	?	?
- new approaches to scalability of high-performance computing application codes	?	?
b) Virtualisation		
- ensuring task isolation and optimised resource allocation as well as guaranteeing performance, timing and reliability constraints	?	yes
- virtualisation solutions for heterogeneous multicore platforms, including the design of virtualisation-ready heterogeneous multicore hardware platforms and support for accelerator virtualisation	?	?
c) Customisation		
- reconfigurable, flexible, soft or hybrid architectures and instruction sets	?	yes
- automatic tool-chain generation	?	?
- system modelling and simulation, including performance predictability	yes	yes
- efficient exploration of the customisation space	?	?
- low-power and customisation for power efficiency	?	?
- parallel programming for single-chip multicore architectures	yes	yes
- architectural and system-level reliability techniques to counter increasingly probabilistic behaviour of transistors in lower geometries	?	?
d) Architecture and Technology		
- the impact of next-generation chip fabrication technology on system architectures, tools and compilers	?	?
- implications of 3D stacking	?	yes
- alternative (non von Neumann) models of computation	yes	yes
- to bridge parallel computing architectures and chip fabrication technology	?	?



8. Usefull links and resources

1. ICT Work Programme 2011-2012 (pdf, 779 KB)
http://cordis.europa.eu/pub/fp7/ict/docs/ict-wp-2011-2012_en.pdf
2. Computing Systems home page
http://cordis.europa.eu/fp7/ict/computing/home_en.html
3. Computing Systems Events and Consultation Workshops:
[http:// cordis.europa.eu/fp7/ict/computing/events_en.html](http://cordis.europa.eu/fp7/ict/computing/events_en.html)
4. Computing Systems// Portfolio of FP7 projects, Dir. G: Components and Systems, Unit G3: Embedded Systems and Control.
5. Information and Communications Technologies
<http://cordis.europa.eu/fp7/ict>
6. Practical Guide to EU Funding Opportunities For Research And Innovation
http://cordis.europa.eu/eu-funding-guide/home_en.html

Thank you!